

Figure 1

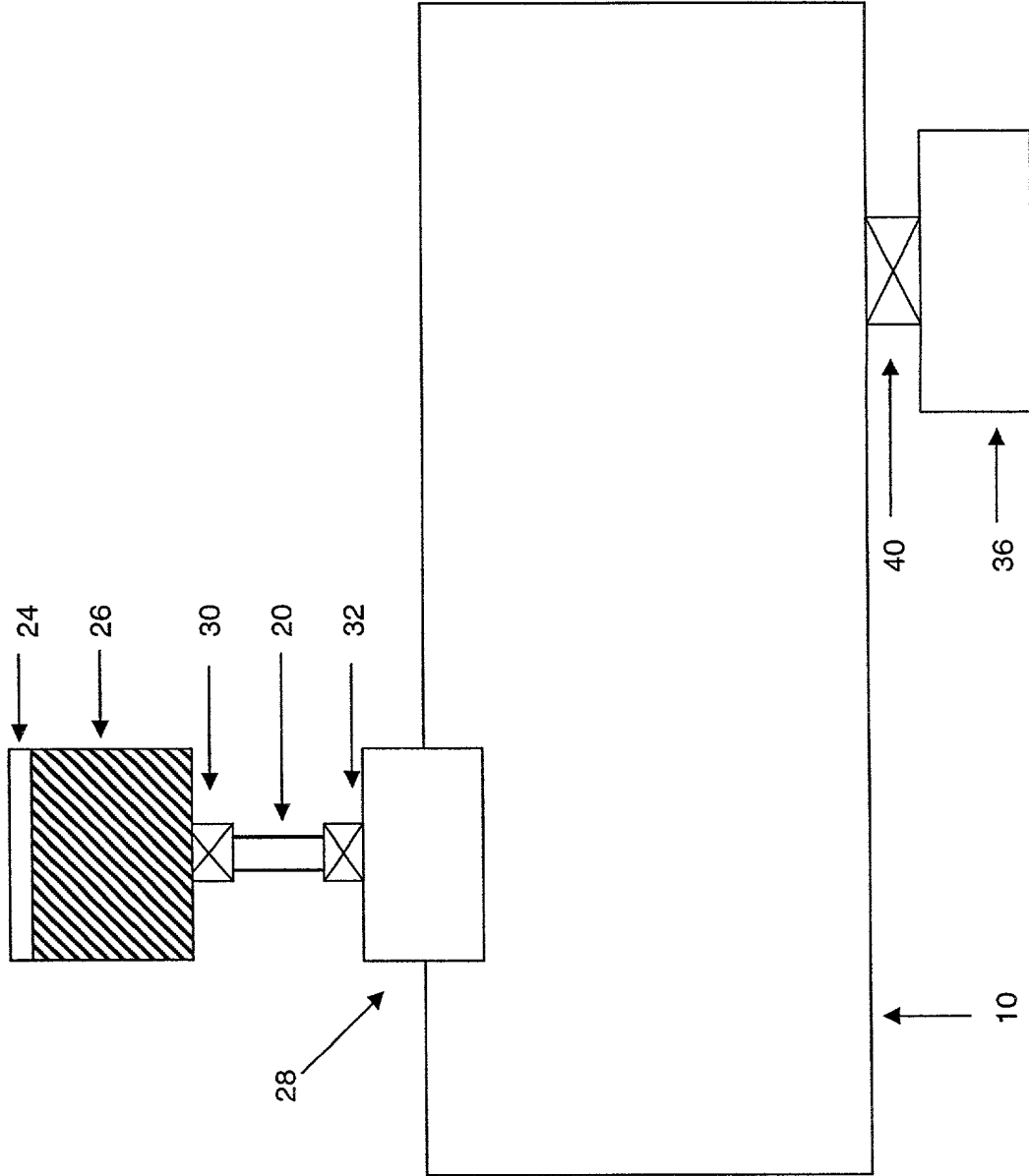


Figure 2A

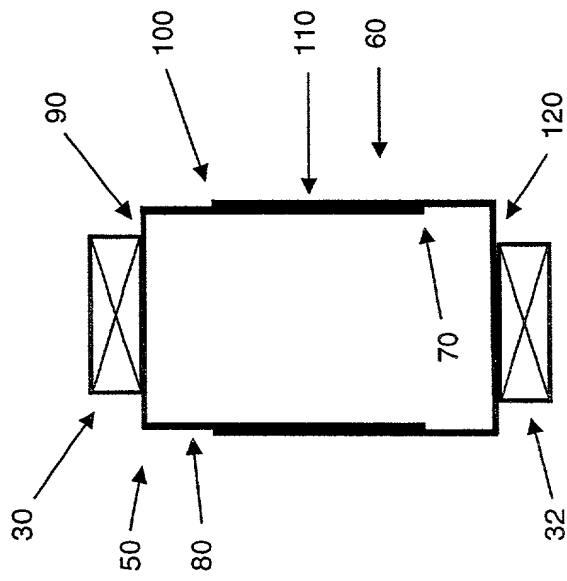


Figure 2B

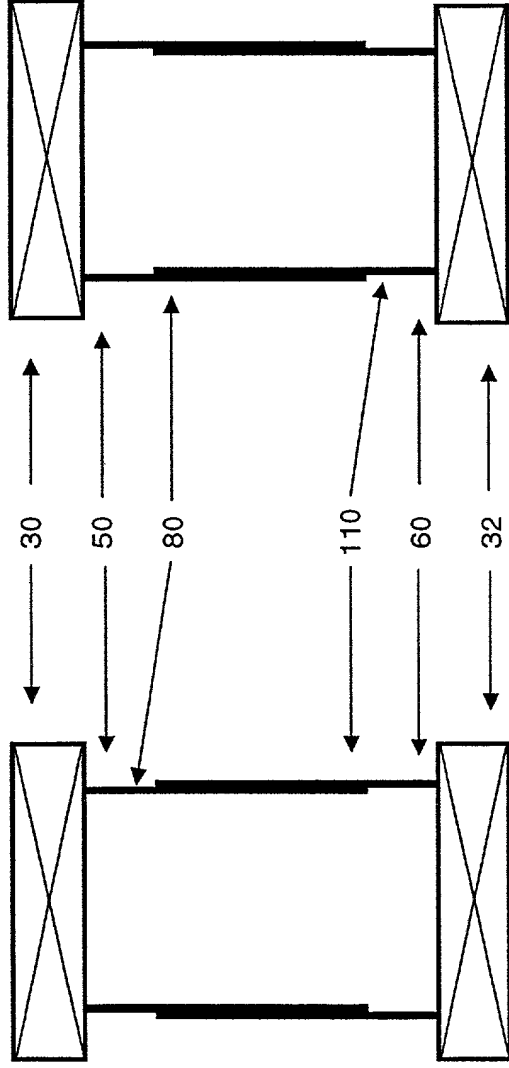


Figure 2C

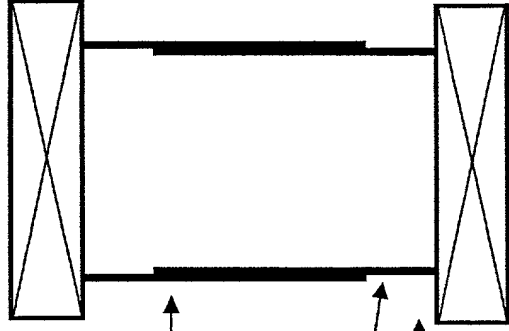


Figure 3A

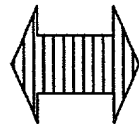


Figure 3B

30

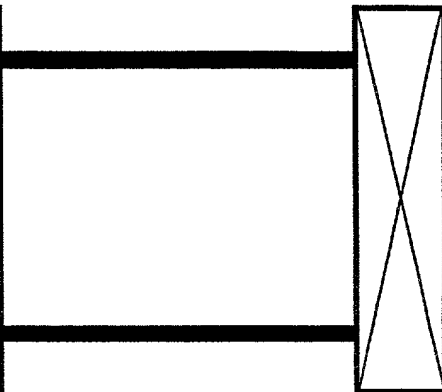
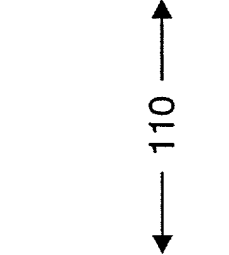


Figure 3C

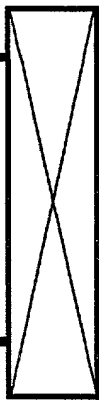


50



110

60



32

This diagram shows a cross-sectional view of a semiconductor device. A central channel (120) is formed in a substrate (130). The channel is lined with a material (180) and has a top layer (60). The channel is flanked by two regions (170) which are also lined with material (180) and have a top layer (60). The device is connected to a source/drain region (24) and a gate region (26) on the left, and a gate region (28) on the right. The channel is connected to a gate region (28) on the right. The channel is connected to a gate region (28) on the right. The channel is connected to a gate region (28) on the right.

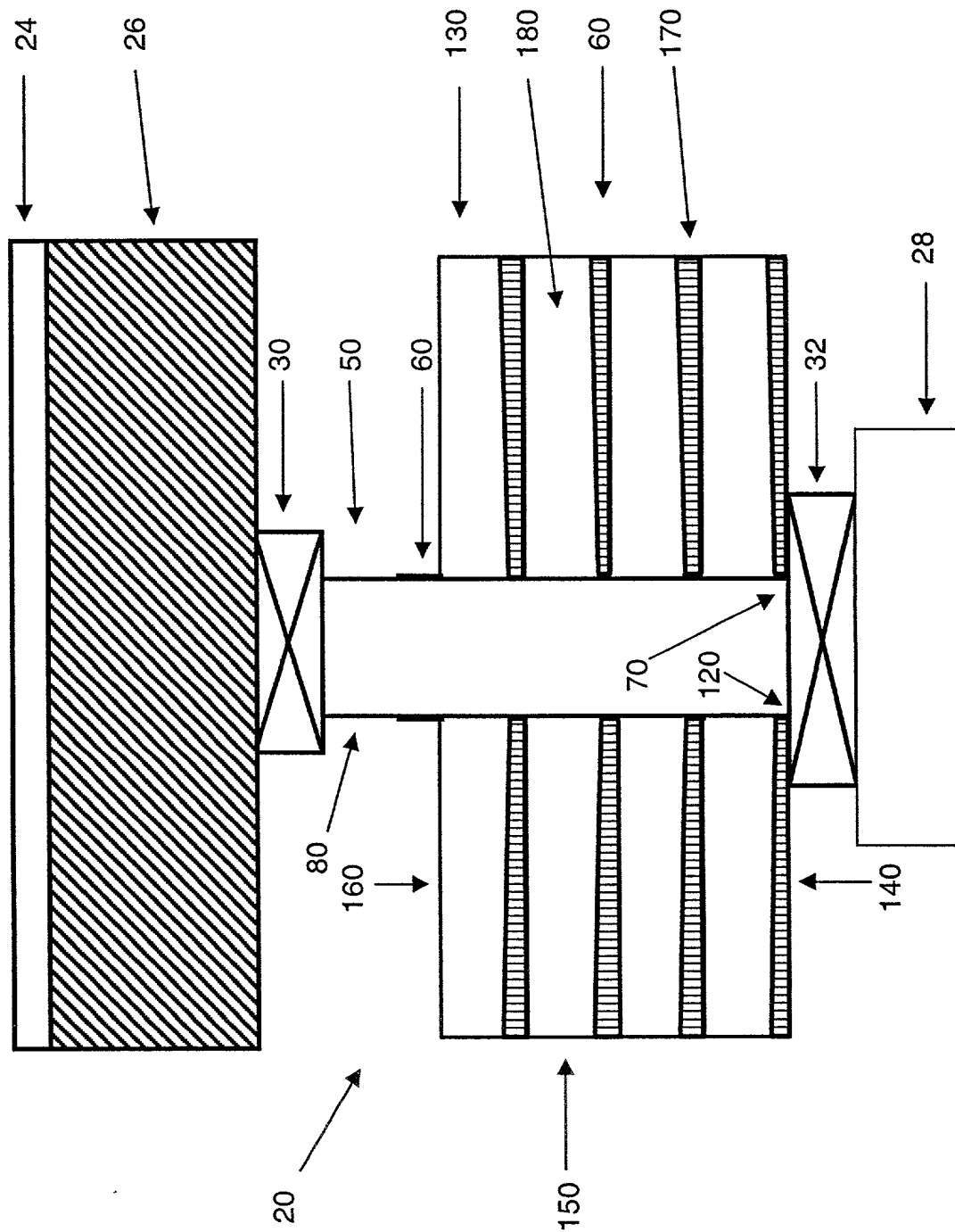


Figure 5

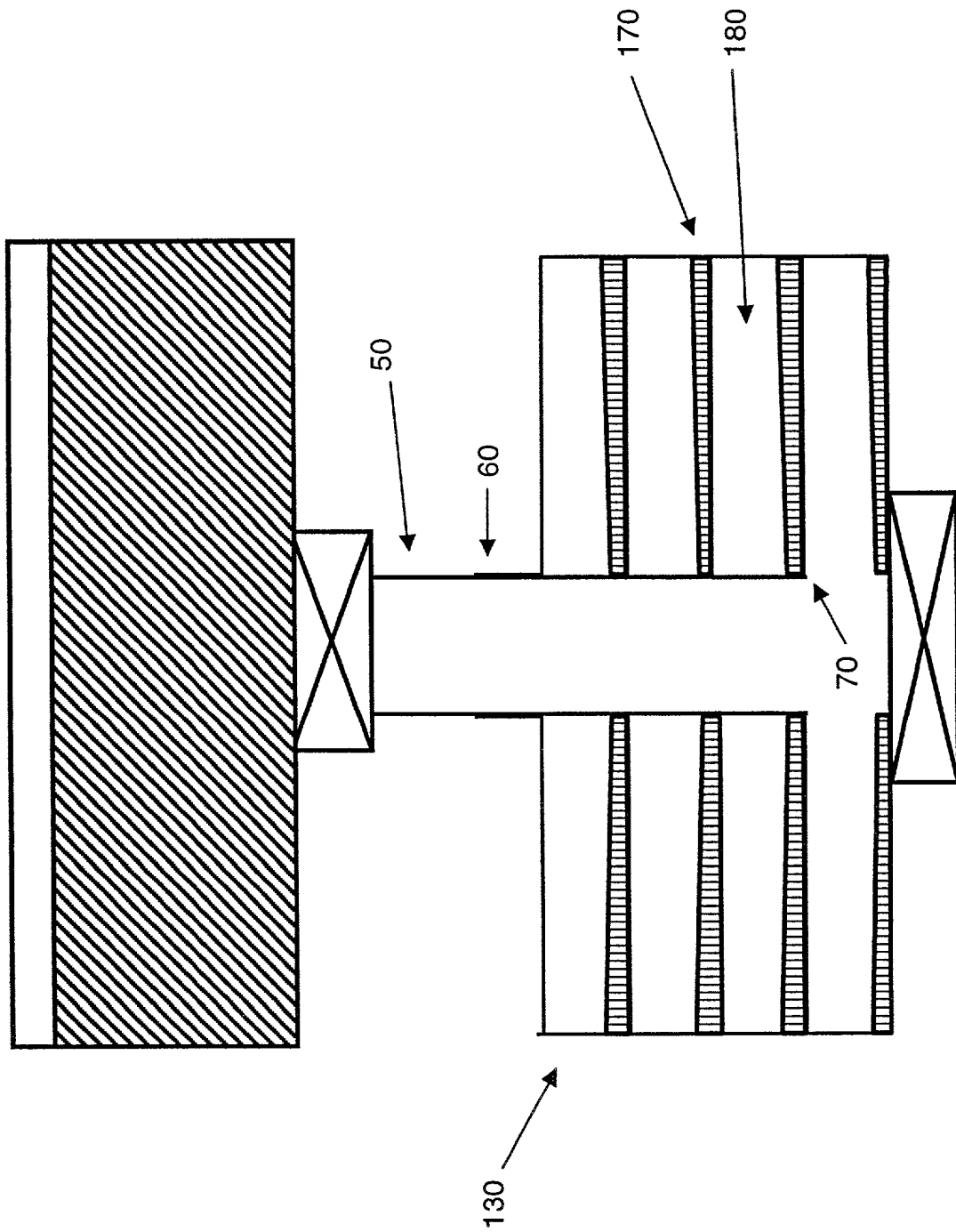


Figure 8

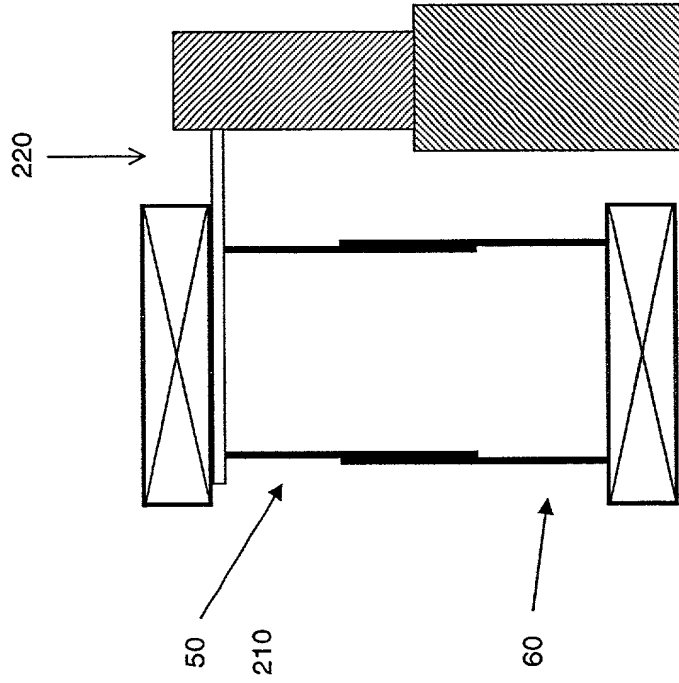


Figure 7

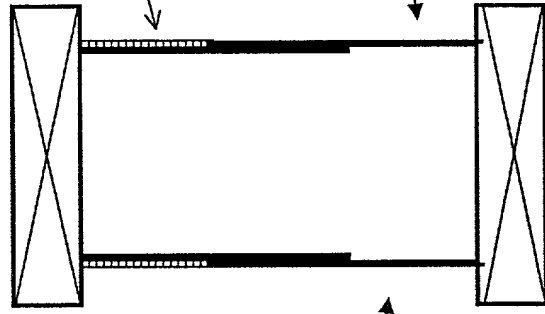


Figure 6

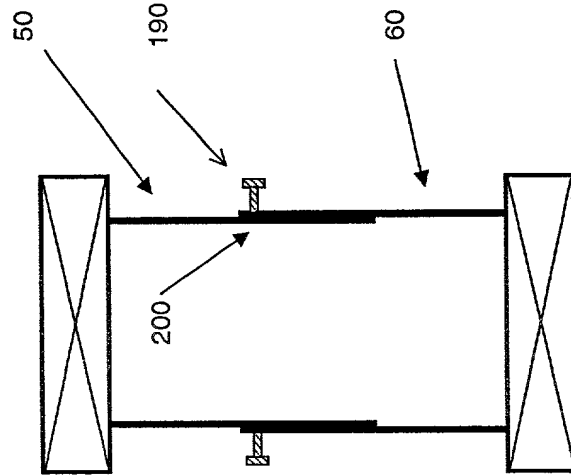


Figure 9

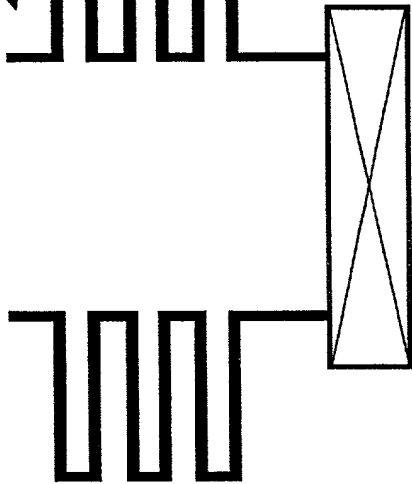


Figure 10

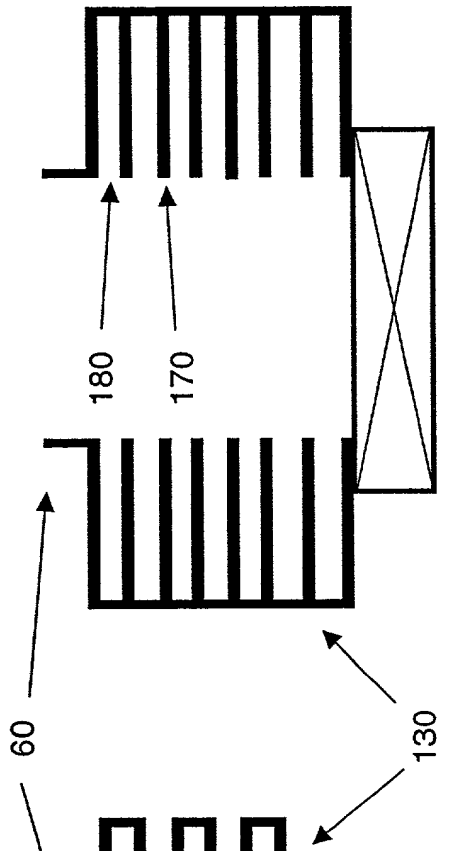


Figure 11

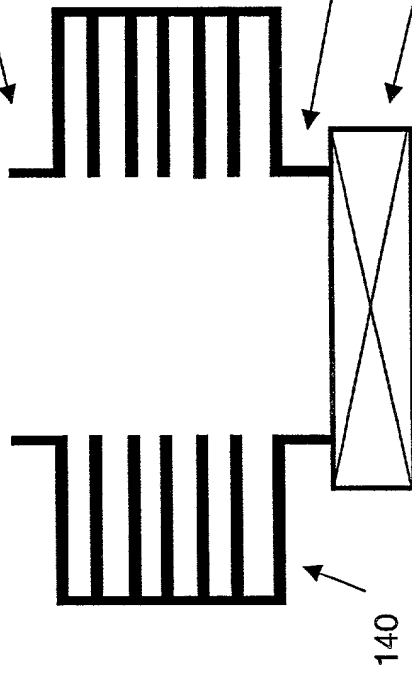


Figure 12

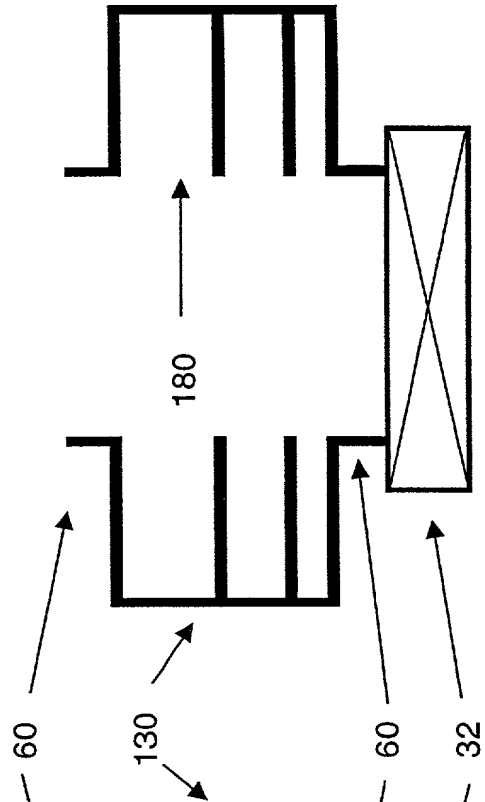


Figure 13

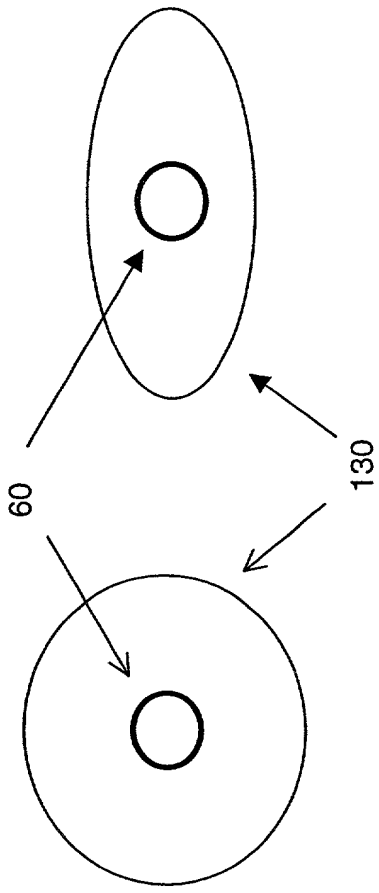


Figure 14

Figure 15

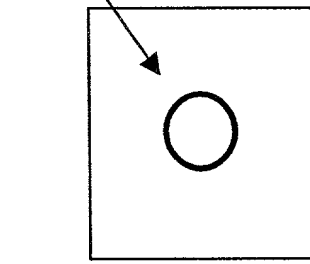


Figure 16

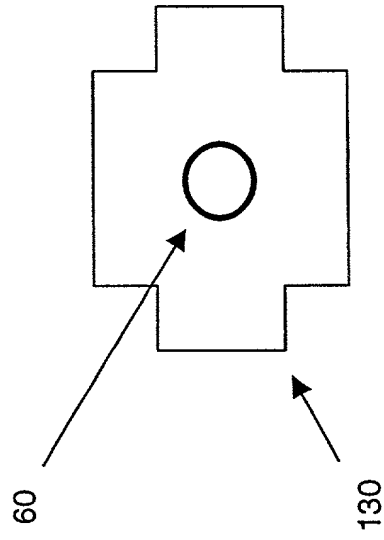




Figure 17

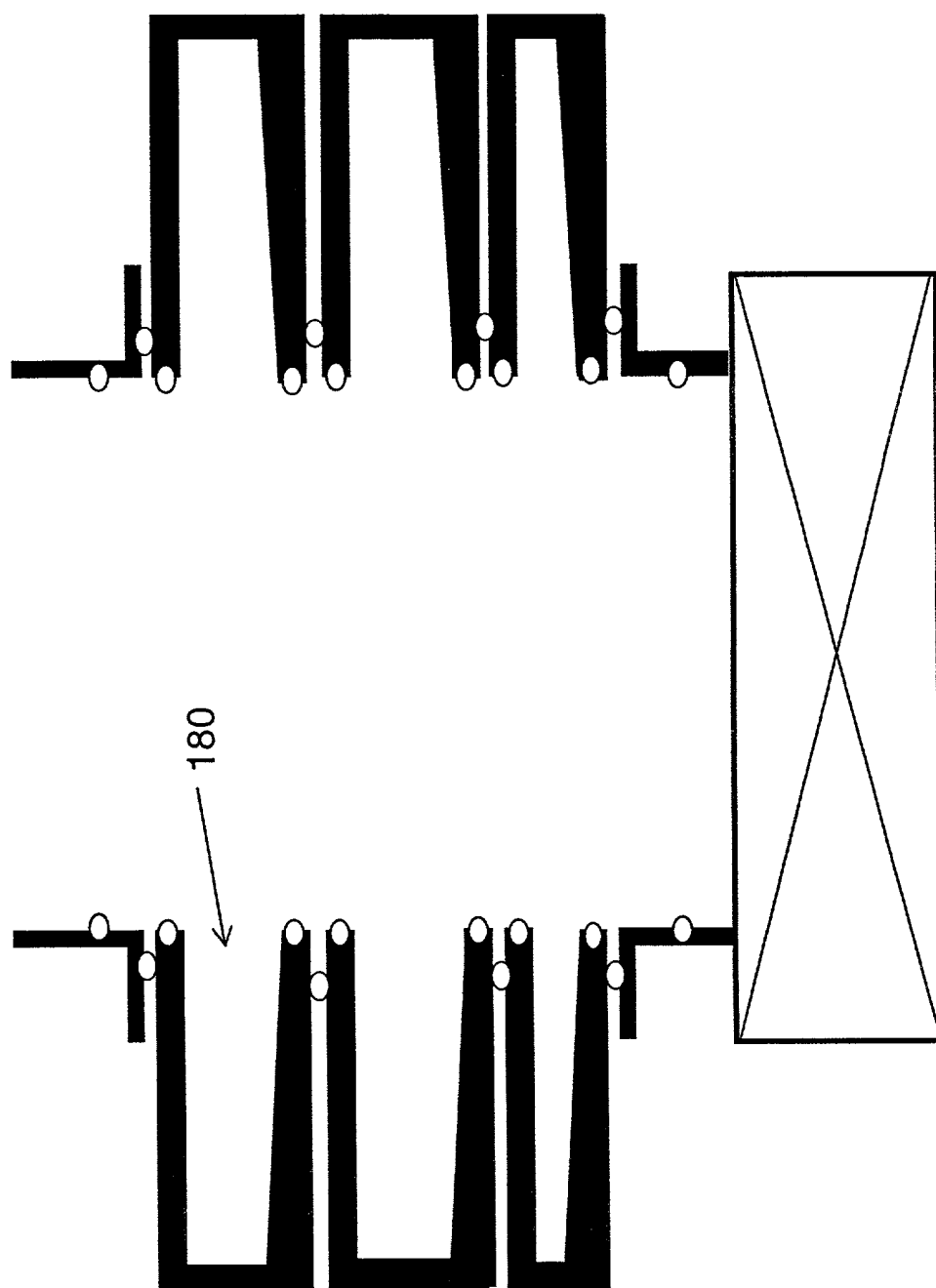


Figure 19

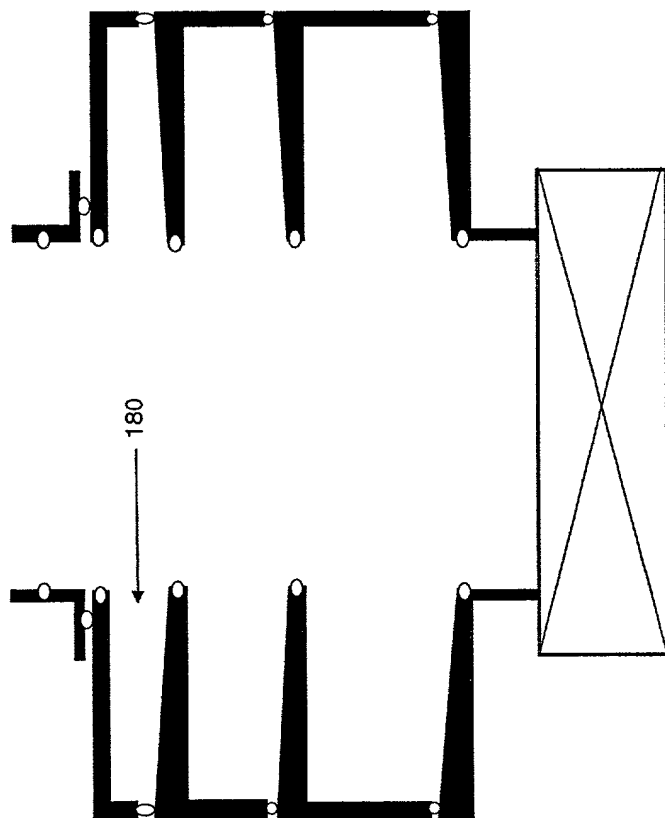


Figure 18

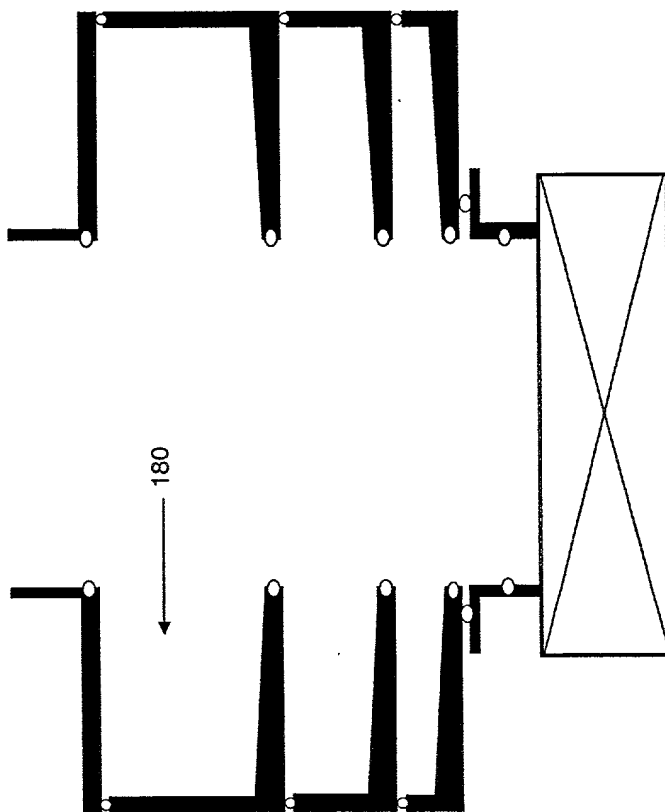


Figure 20

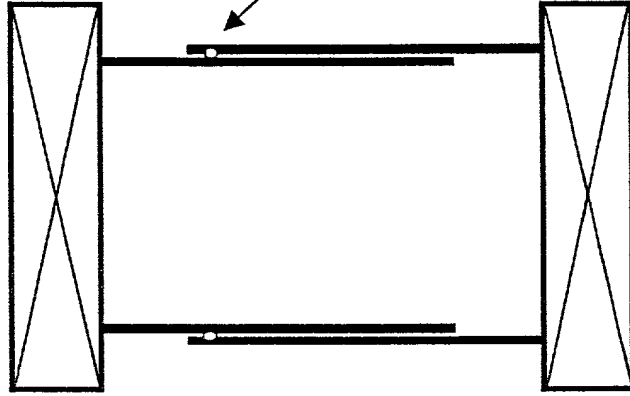


Figure 21

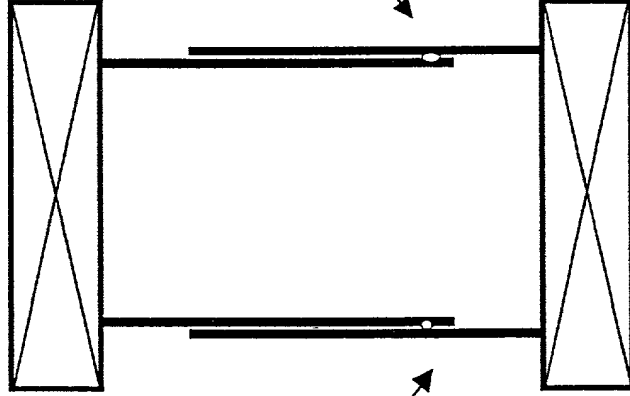


Figure 22

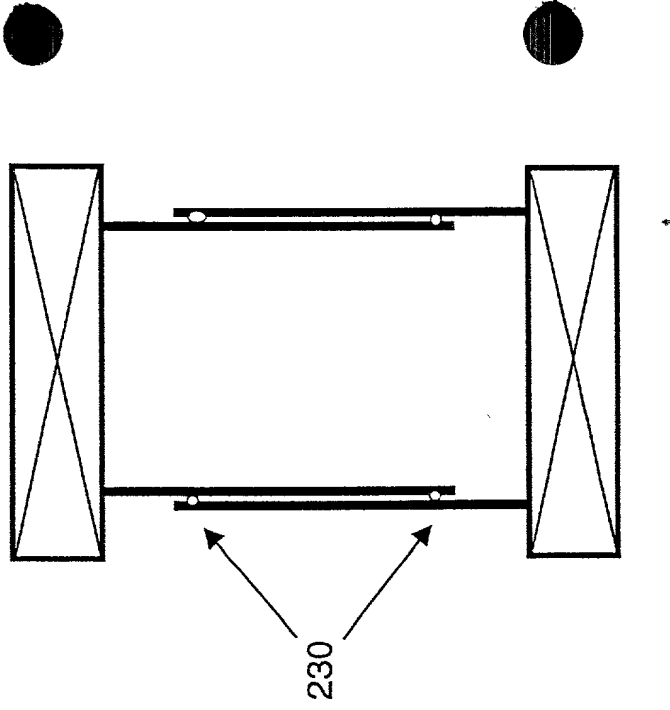
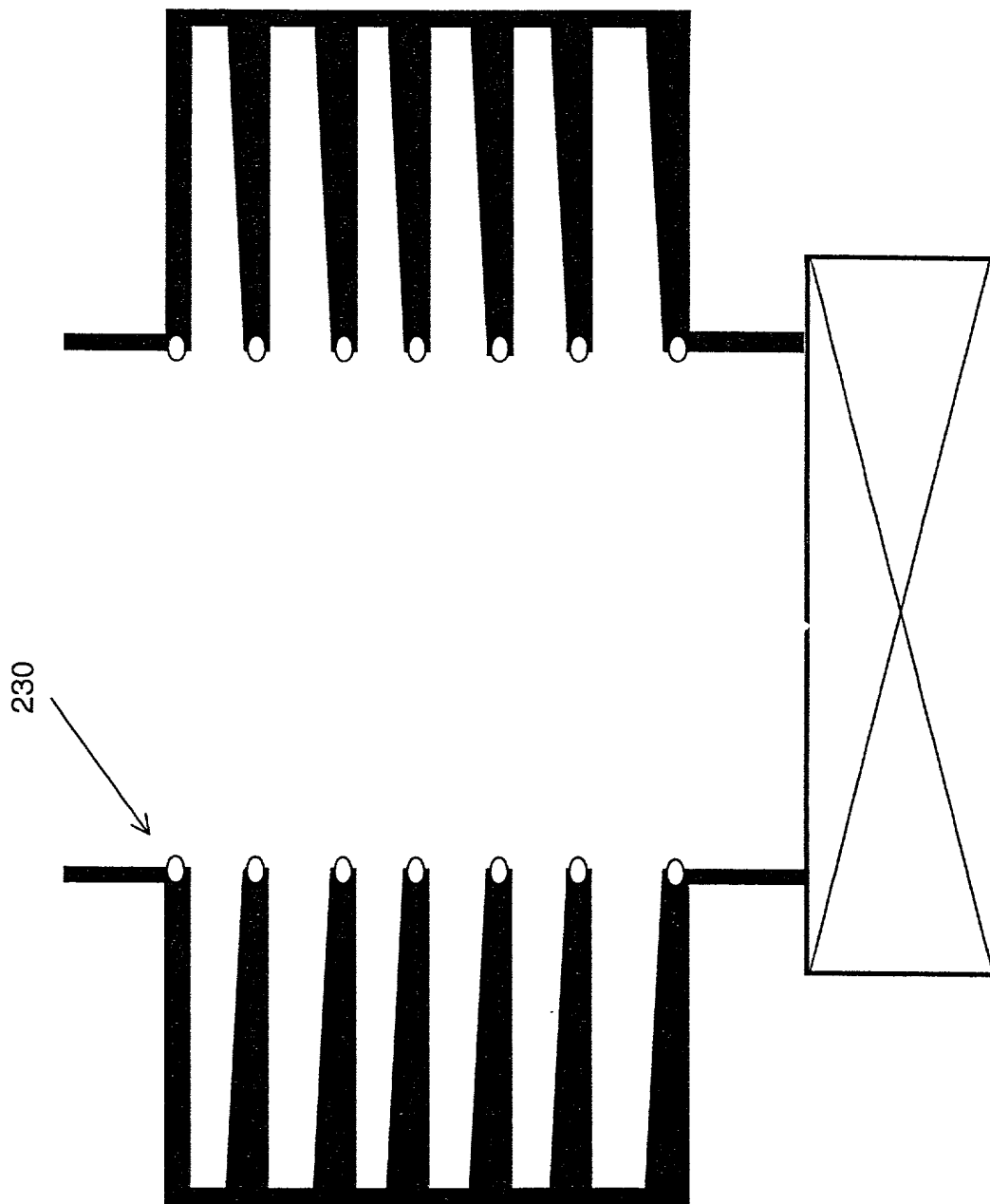
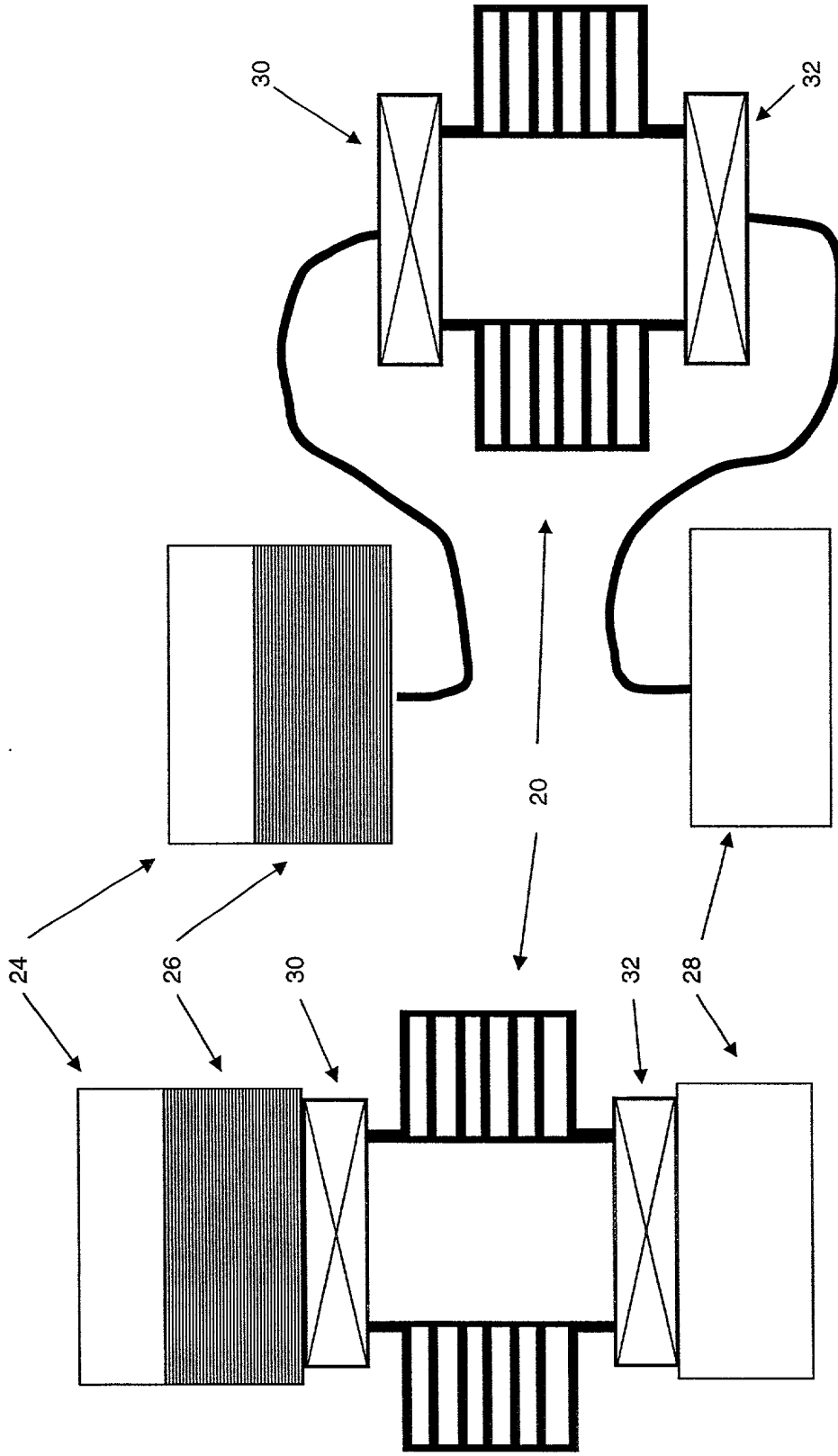


Figure 23



**Figure 24**



**Figure 25**

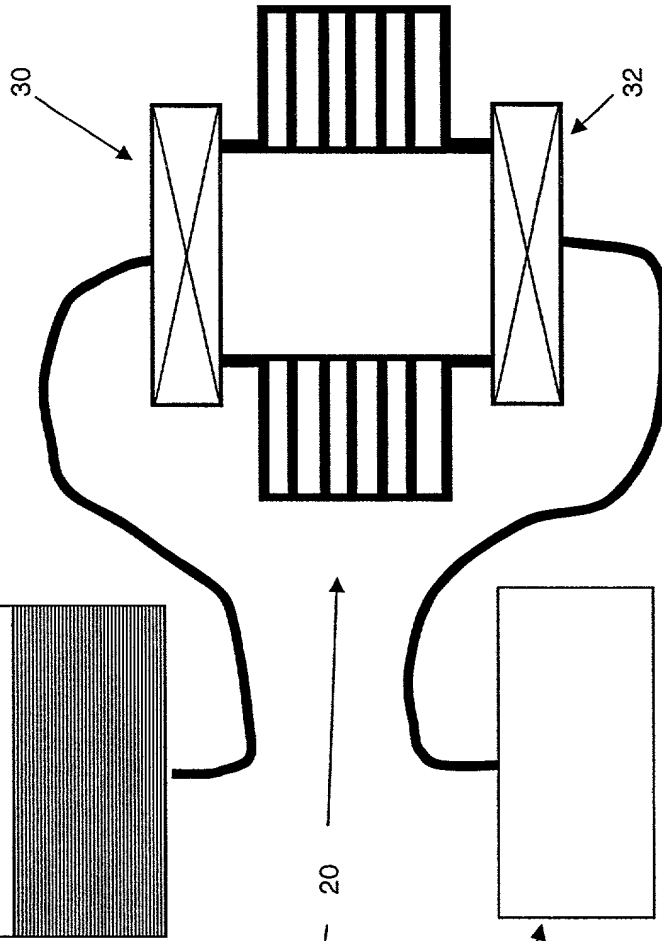


Figure 26

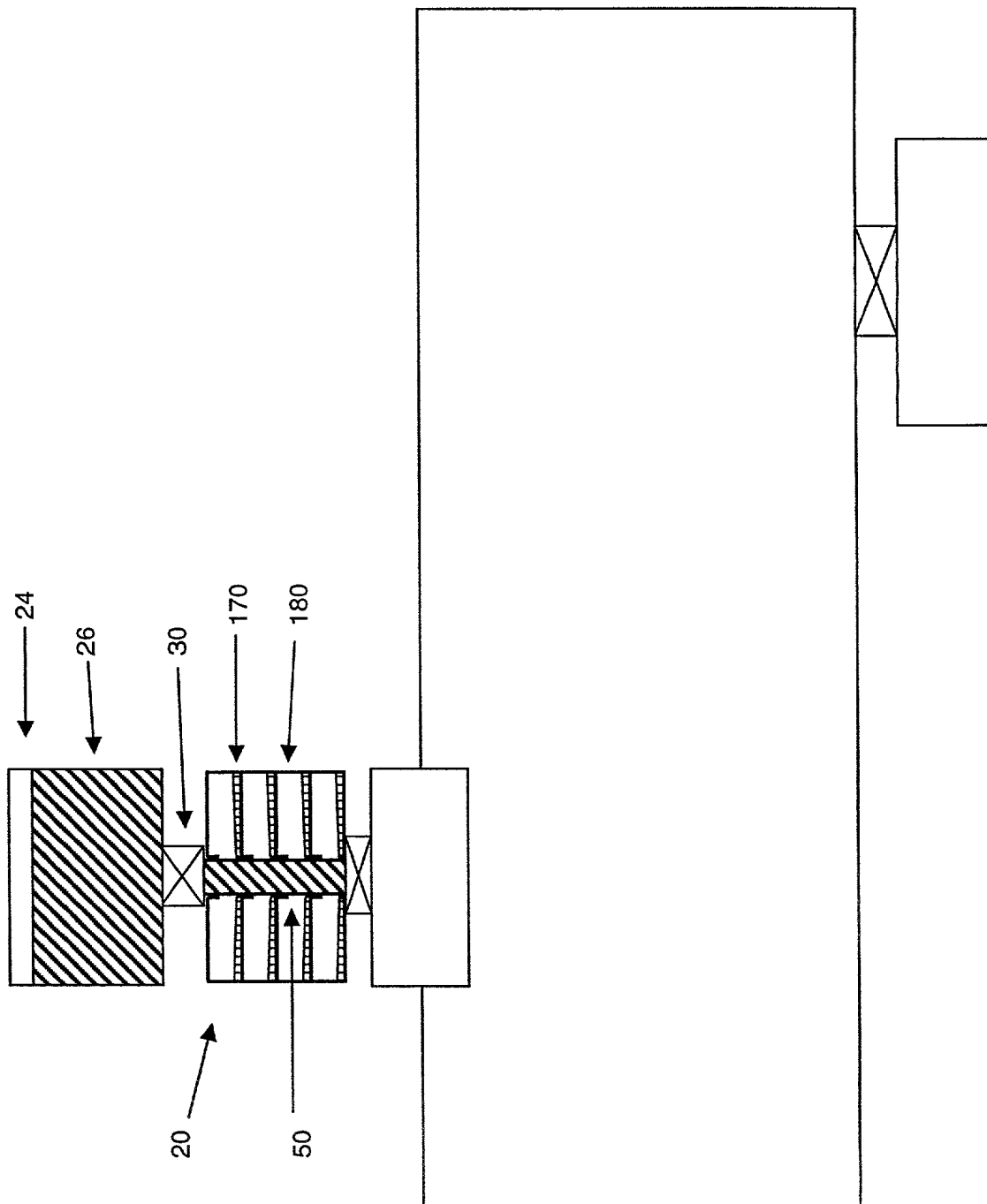
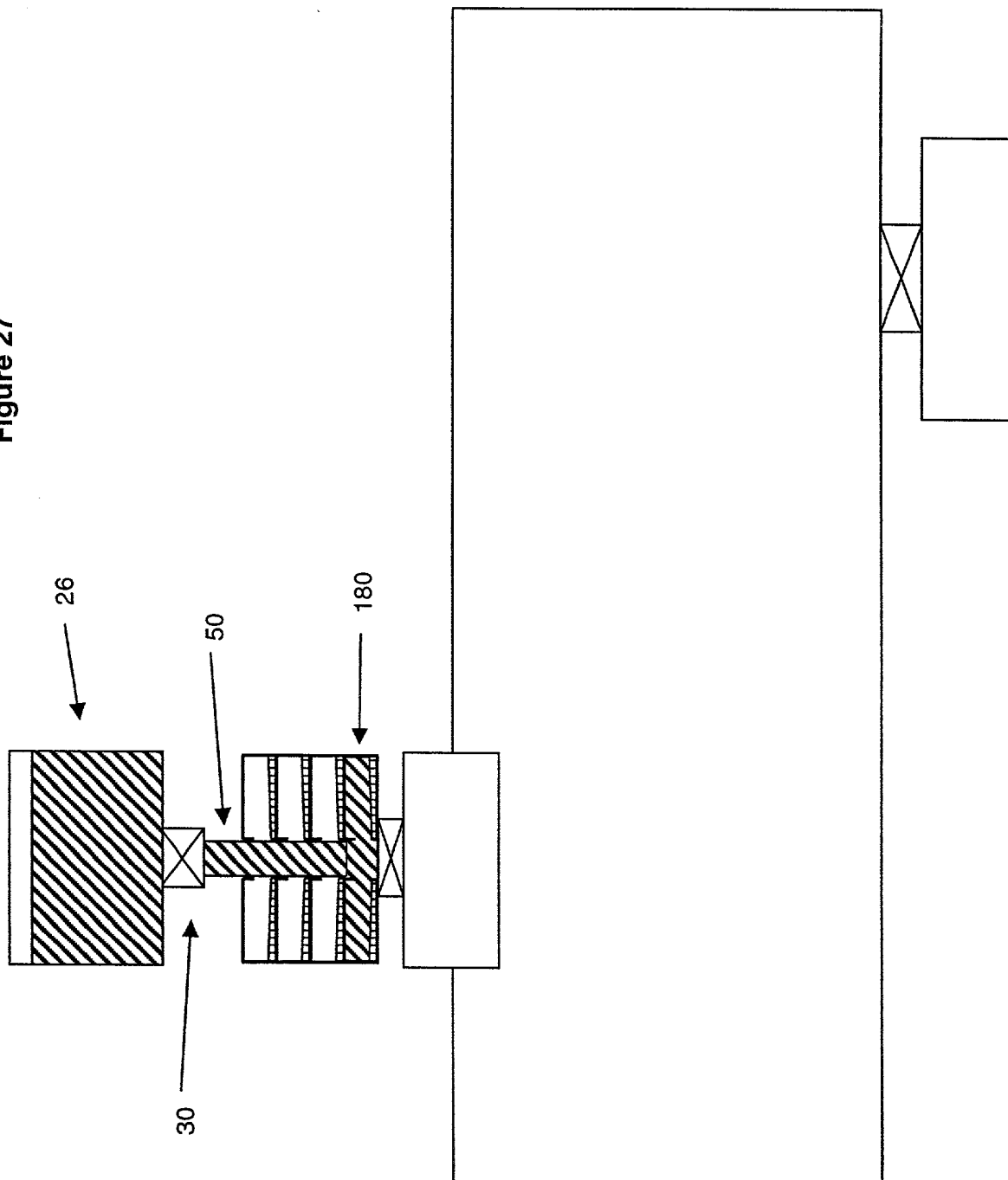


Figure 27



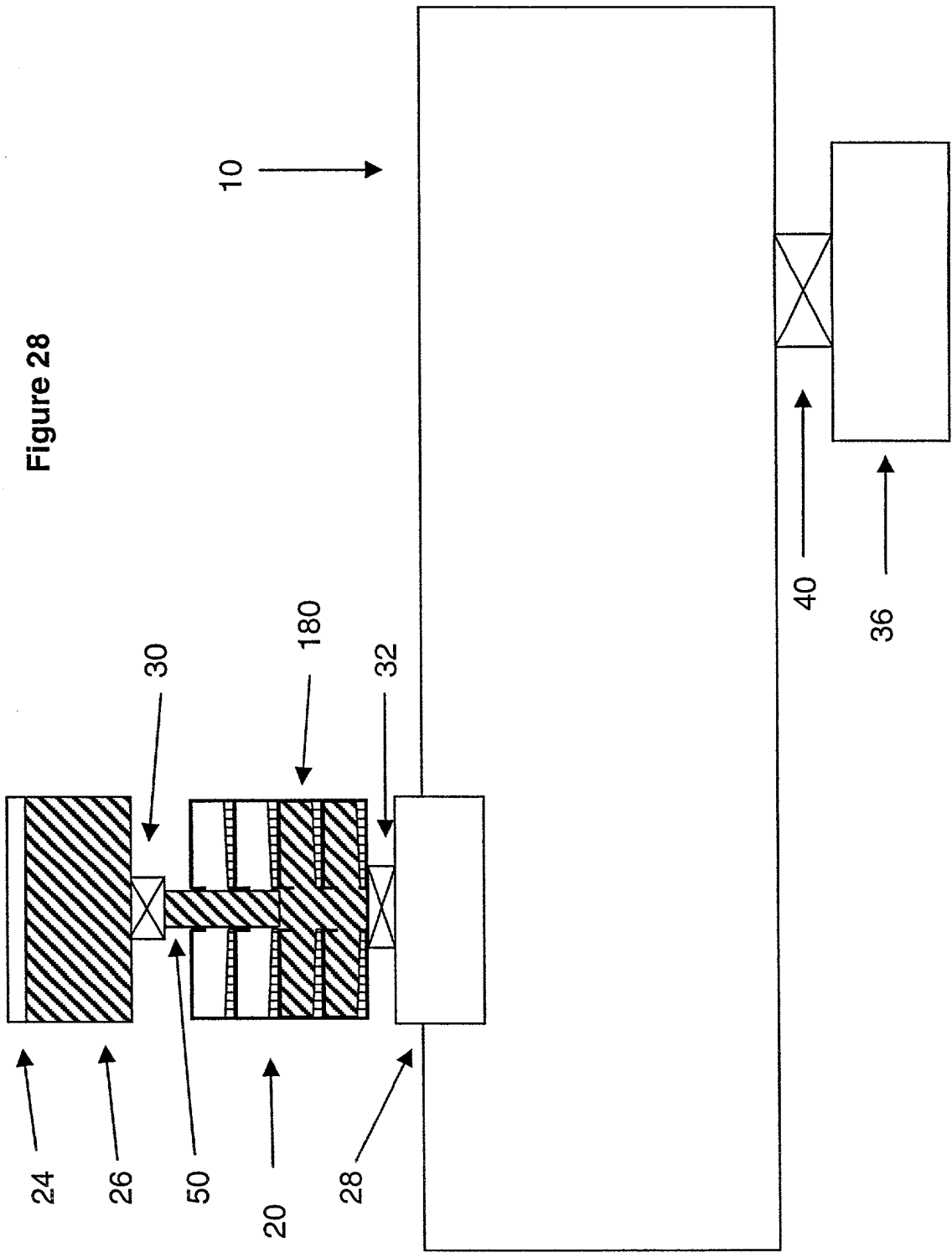


Figure 28